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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,350	12/12/2001	Jason Gonzalez	10010983-1	8391

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AGILENT TECHNOLOGIES, INC.  
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EXAMINER

JONES, STEPHEN E

ART UNIT

PAPER NUMBER

2817

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/015,350

Applicant(s)

GONZALEZ ET AL.

Examiner

Stephen E. Jones

Art Unit

2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_.  
2a) This action is FINAL.      2b) This action is non-final.  
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.  
5) Claim(s) \_\_\_\_ is/are allowed.  
6) Claim(s) 1-6, 13-17 and 20 is/are rejected.  
7) Claim(s) 7-12, 18 and 19 is/are objected to.  
8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.  
10) The drawing(s) filed on 12 December 2001 is/are: a) accepted or b) objected to by the Examiner.  
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
11) The proposed drawing correction filed on \_\_\_\_ is: a) approved b) disapproved by the Examiner.  
    If approved, corrected drawings are required in reply to this Office action.  
12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All b) Some \* c) None of:  
    1. Certified copies of the priority documents have been received.  
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.  
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
    a) The translation of the foreign language provisional application has been received.  
15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) Notice of References Cited (PTO-892)  
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_ .  
4) Interview Summary (PTO-413) Paper No(s) \_\_\_\_ .  
5) Notice of Informal Patent Application (PTO-152)  
6) Other: \_\_\_\_ .

**DETAILED ACTION*****Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the additional driver in Claims 7-12 and 18-19 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-6, 13-15, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Mughal et al.

Mughal teaches an impedance matching circuit including: an external impedance ( $Z$ ) (i.e. a load impedance) between an external contact (pad 26) and a first source potential (i.e. ground); inherently the load impedance includes the impedance of the interconnection of the pad (26) connected to the output terminal of a driver in the same

configuration as the present invention; an adjustable impedance is formed by MOSFET's (W1, W2, etc.) which are connected between a second source potential (Vdd) and the output of the driver in the same configuration as the present invention (Claims 3, 15); a reference potential is Vdd/2 obtained by the resistor divider formed by two equal resistors (R1) (Claims 5, 17); and a controller (32) changes the adjustable impedance by switching the transistors either on or off individually to obtain a desired matched impedance which thus inherently results in matching the reference voltage and output of the driver to within a particular pre-selected difference (see Col. 4, lines 1-4) (Claims 1-2, 6, 13, 14).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mughal et al.

Mughal teaches an impedance matching circuit as described above. However, Mughal does not explicitly teach that the first potential is the supply potential and the second source potential is the ground potential.

It would have been considered obvious to one of ordinary skill in the art to have switched/reversed the ground node and source node in the Mughal circuit, because the selection of ground potential is an arbitrary selection of the reference node as would have been known to one of ordinary skill in the art.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mughal et al. in view of Fujimura et al.

Mughal et al. teaches an impedance matching circuit as described above. However, Mughal does not explicitly teach an open circuit detector circuit which is capable of detecting an open circuit at the external contact.

Fujimura teaches that it is conventional to use an open circuit detection circuit at a load connection to detect when a load is not connected.

It would have been considered obvious to one of ordinary skill in the art to have included a well-known open circuit detection circuit at the load connection such as taught Fujimura in the Mughal circuit, because it would have provided the advantageous benefit of a means for signaling the controller when no load is present such that the controller would not continue to switch the transistors to match the infinite impedance of the open circuit caused by the no-load condition, thereby suggesting the obviousness of

such a modification. Also, note that the controller would still have been "capable" of adjusting the impedance to a pre-selected value when an open circuit was detected.

***Allowable Subject Matter***

8. Claims 7-12 and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach that the conducting traces have different length to width ratios and the load matching impedance is selected based on the conducting trace length to width ratio of an additional driver (Claims 7-9), or based on the conducting length and width of the driver and an additional driver computing the load matching impedance which provides the closest match of the output impedance to the load impedance of the additional driver (Claims 10-12 and 18-19).

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dunlop et al. teaches a digitally controlled impedance circuit.

Claridge et al. teaches an automatic impedance matching circuit.

Hayt et al. (Engineering Circuit Analysis) teaches the general concept of selecting two nodes in a circuit network to define a voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen E. Jones whose telephone number is 703-305-0390. The examiner can normally be reached on Monday through Friday from 8 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 703-308-4909. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

  
Stephen Jones  
Patent Examiner  
Art Unit 2817

SEJ